

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-13. (Cancelled)

14. (New) A storage controller, comprising:

a first memory that stores a plurality of data blocks that include first and second noncontiguous data segments;

a queue module that stores data lengths and data start addresses of the first and second data segments; and

a read assembly module that communicates with the first memory and the queue module, that receives a request to read the first and second data segments from a host, that reads the plurality of data blocks from the first memory based on the data lengths and data start addresses, that extracts the first and second data segments from the plurality of data blocks, and that transfers the first and second data segments contiguously to the host.

15. (New) The storage controller of claim 14 wherein the plurality of data blocks include data integrity verification data.

16. (New) The storage controller of claim 15 wherein the data integrity verification data is cyclic redundancy code (CRC) data.

17. (New) The storage controller of claim 15 wherein the read assembly module does not transfer the data integrity verification data to the host.

18. (New) The storage controller of claim 14 wherein the read assembly module concatenates the first and second data segments.

19. (New) The storage controller of claim 14 further comprising a second memory, wherein the read assembly module transfers the first and second data segments to the second memory and the second memory transfers the first and second data segments to the host.

20. (New) The storage controller of claim 19 wherein the second memory is a first in first out (FIFO) buffer.

21. (New) The storage controller of claim 14 wherein the first memory is a buffer memory.

22. (New) The storage controller of claim 21 wherein the buffer memory receives the first and second data segments from a storage device.

23. (New) The storage controller of claim 22 wherein the storage device is a hard disk drive (HDD).

24. (New) A storage controller, comprising:

first memory means for storing a plurality of data blocks that include first and second noncontiguous data segments;

queue means for storing data lengths and data start addresses of the first and second data segments; and

read assembly means for communicating with the first memory and the queue module, for receiving a request to read the first and second data segments from a host, for reading the plurality of data blocks from the first memory based on the data lengths and data start addresses, for extracting the first and second data segments from the plurality of data blocks, and for transferring the first and second data segments contiguously to the host.

25. (New) The storage controller of claim 24 wherein the plurality of data blocks include data integrity verification data.

26. (New) The storage controller of claim 25 wherein the data integrity verification data is cyclic redundancy code (CRC) data.

27. (New) The storage controller of claim 25 wherein the read assembly means does not transfer the data integrity verification data to the host.

28. (New) The storage controller of claim 24 wherein the read assembly means concatenates the first and second data segments.

29. (New) The storage controller of claim 24 further comprising second memory means for storing data, wherein the read assembly means transfers the first and second data segments to the second memory means and the second memory means transfers the first and second data segments to the host.

30. (New) The storage controller of claim 29 wherein the second memory means is a first in first out (FIFO) buffer.

31. (New) The storage controller of claim 24 wherein the first memory means receives the first and second data segments from a storage device.

32. (New) The storage controller of claim 31 wherein the storage device is a hard disk drive (HDD).

33. (New) A method for operating a storage controller, comprising:

- storing a plurality of data blocks that include first and second noncontiguous data segments in a first memory;
- storing data lengths and data start addresses of the first and second data segments in a queue module;
- receiving a request to read the first and second data segments from a host at a read assembly module;
- reading the plurality of data blocks from the first memory based on the data lengths and data start addresses;
- extracting the first and second data segments from the plurality of data blocks; and
- transferring the first and second data segments contiguously to the host.

34. (New) The method of claim 33 wherein the plurality of data blocks include data integrity verification data.

35. (New) The method of claim 34 wherein the data integrity verification data is cyclic redundancy code (CRC) data.

36. (New) The method of claim 34 wherein the read assembly module does not transfer the data integrity verification data to the host.

37. (New) The method of claim 33 further comprising concatenating the first and second data segments.

38. (New) The method of claim 33 further comprising:
transferring the first and second data segments from the read assembly module to a second memory; and
transferring the first and second data segments from the second memory to the host.

39. (New) The method of claim 38 wherein the second memory is a first in first out (FIFO) buffer.

40. (New) The method of claim 33 further comprising receiving the first and second data segments from a storage device.

41. (New) The method of claim 40 wherein the storage device is a hard disk drive (HDD).